The complexity of circuit values, network flows, and matchings

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Background

Our project was centered around narrowing the classification of the Bipartite Perfect Matching problem (BPM), with the long-term goal being to succinctly describe a complexity class for which BPM is complete. Our attempts to resolve this were based on the relations between BPM and two other well-known problems, Network Flow and Boolean Circuit Value.

Bipartite Perfect Matching

The Bipartite Perfect Matching problem is one of determining given a bipartite graph G whether there exists a perfect matching on G.

Network Flow

For our purposes, the Network Flow problem was the problem of deciding, given a flow network G and an integer i, whether the i-th bit in the maximum flow value of G is one. We distinguished between the cases where the capacities of G are specified in unary or in binary.

Boolean Circuit Value

We considered a restriction of the Boolean Circuit Value problem to the case where the circuits are monotone (i.e., contain only AND gates, OR gates, and constants) and each gate has a fan-out of exactly two. Goldschlager established in [1] that this restriction does not reduce the complexity of the problem.

Relating the Problems

In [1], Goldschlager showed that the Boolean Circuit Value problem is equivalent under logspace reductions to the Network Flow Problem when the capacities are expressed in binary (they are both complete for P). Further, it is known that BPM is similarly equivalent to Network Flow with capacities in unary.

The Goal

Our aim was to either modify Goldschlager's reduction from Circuit Value to allow the capacities to be expressed in unary (while still using only a logarithmic amount of space) or to develop a class of circuits which would admit a similar reduction. The latter would allow us to describe a natural complexity class for BPM in terms of circuits.

The Main Obstacle

Under the reductions we were examining, each gate in our circuit mapped to a single node in the corresponding flow network. When the gate evaluated to true, the flow along the edges leaving the node would equal the capacities along those edges; when the gate evaluated to false, the flow out would be zero.

With this model, the capacities of the edges leading into each node would need to be double the capacities leading out (ignoring edges toward the source and sink). Thus, the capacities would have to grow exponentially in their distance from the sink, preventing us from expressing them in unary in log space.

Differentiating AND and OR

Initially, this problem seemed to be inherent only to OR gates, so we tried to modify how the AND gates mapped to nodes in the resulting flow network. Unfortunately, we discovered a strong duality in the way the two types of gate behaved under the transformation, which prevented us from improving the rate at which the capacities grow.

Modeling Other Gates

Next, we looked at modeling gates other than AND gates and OR gates. First, we attempted to model NOT or XOR gates in an attempt to relax the monotonicity requirement. We observed that non-monotone gates cannot be modeled by single nodes in a flow network without breaking the conservation of flow. This led us to conjecture that only linearly separable functions can be modeled by individual nodes.

Fig 1. AND gate

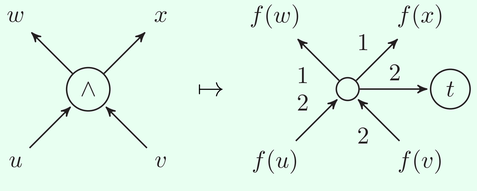
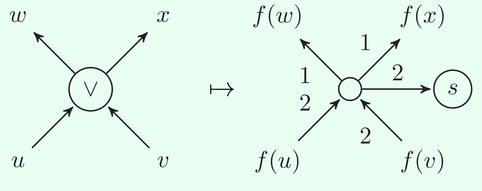


Fig 2. OR gate



Further Research

- There may be a circuit model using nonconventional gates which reduces more readily to the Unary Network Flow problem.
- BPM may be reducible to a stability problem in flow networks with feedback.
- It may be possible to reduce BPM to the Lexicographically-first Maximal Matching problem.
- Perhaps the reduction from BPM to Unary Network Flow could be adapted to produce a reduction from the succinct version of BPM to Binary Network Flow.

References

[1] Goldschlager, L.M., Shaw, R.A., and Staples, J. The Maximum Flow Problem is Log Space Complete for P. In *Proceedings of Theor. Comput. Sci.*. 1982, 105-111.

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